



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: CYPR-CD01167M

Inventor(s): Bartz et al.

Application No.: 09/989,570

Group Art Unit:

Filed: 11/19/01

Examiner:

Title: METHOD FOR FACILITATING MICROCONTROLLER PROGRAMMING

Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

| <u>Pat. No.</u> | <u>Pat. Title</u> | <u>Grant Date</u> |
|-----------------|--|-------------------|
| 5,930,148 | METHOD AND SYSTEM FOR VERIFYING A DIGITAL CIRCUIT DESIGN INCLUDING DYNAMIC CIRCUIT CELLS THAT UTILIZE DIVERSE CIRCUIT TECHNIQUES | 07/27/99 |
| 6,571,373 | SIMULATOR-INDEPENDENT SYSTEM-ON-CHIP VERIFICATION METHODOLOGY | 05/27/03 |
| 6,615,167 | PROCESSOR-INDEPENDENT SYSTEM-ON-CHIP VERIFICATION FOR EMBEDDED PROCESSOR SYSTEMS | 09/02/03 |
| 6,052,524 | SYSTEM AND METHOD FOR SIMULATION OF INTEGRATED HARDWARE AND SOFTWARE COMPONENTS | 04/18/00 |

The Examiner's attention is respectfully directed to the following U.S. Patent Application Publication:

| <u>Pub. No.</u> | <u>Pub. Title</u> | <u>Pub. Date</u> |
|-----------------|--|------------------|
| 2003/0163798 | METHOD AND SYSTEM FOR INTEGRATING CORES IN FPGA-BASED SYSTEM-ON-CHIP (SOC) | 08/28/03 |

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP

Two North Market Street, Third Floor


San Jose, California 95113

(408) 938-9060

Customer No: 45545

Respectfully submitted,

Date: 10/25/04

By: 
Ronald M. Pomerence
Reg. No. 43,009



Attorney Docket No.: CYPR-CD01167M.....

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Patent Application

Inventor(s): Bartz et al.

Application No.: 09/989,570

Group Art Unit:

Filed: 11/19/01

Examiner:

Title: METHOD FOR FACILITATING MICROCONTROLLER PROGRAMMING

Form 1449

U.S. Patent Documents

| Examiner Initial | No. | Patent No. | Date | Patentee | Class | Sub-class | Filing Date |
|------------------|-----|------------|----------|------------------|-------|-----------|-------------|
| | A | 5930148 | 07/27/99 | Bjorksten et al. | 364 | 488 | 12/16/96 |
| | B | 6571373 | 05/27/03 | Devins et al. | 716 | 5 | 01/31/00 |
| | C | 6615167 | 09/02/03 | Devins et al. | 703 | 28 | 01/31/00 |
| | D | 6052524 | 04/18/00 | Pauna | 395 | 500.43 | 05/14/98 |

U.S. Patent Application Publication

| Examiner Initial | No. | Pub. No. | Date | Applicant | Class | Sub-class | Filing Date |
|------------------|-----|----------|------|-----------|-------|-----------|-------------|
| | E | | | | | | |

Foreign Patent or Published Foreign Patent Application

| Examiner Initial | No. | Document No. | Publication Date | Country or Patent Office | Class | Sub-class | Translation | |
|------------------|-----|--------------|------------------|--------------------------|-------|-----------|-------------|----|
| | F | | | | | | Yes | No |
| | | | | | | | | |

Other Documents

| Examiner Initial | No. | Author, Title, Date, Place (e.g. Journal) of Publication |
|------------------|-----|--|
| | G | |
| Examiner | | Date Considered |

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.